Tanat University | Department: Computer and control engineering | Faculty of Engineering

Title: Data Structures and Algorithms
Final exam, Date: 12/1/2014, **Total marks:** 100
Course code: CCE2106
Allowed time: 3 hours
Year: Second year
Number of pages: 2

Workout the following questions

1) Mark each of the following statements as either *true* or *false*. In case of false statement, give the correction *(10 Marks)*
   a) In .NET framework, the array is a dynamic data structure that extended automatically as needed
   b) In data structure sense, direct access means that an element can be reached in a time that is directly depend on its position.
   c) Stack is a linear data structure
   d) The POP operation on a stack retrieves the top element of the stack and removes it from the stack
   e) Peaking a stack means to retrieve the maximum value stored in it
   f) To conserve it's state, a computer processor store it in queue data structure when asked to go away to do something then return back to complete its work
   g) The natural data structure choice for a file system is Trees
   h) As the degree of unbalance in a binary search tree increases as its advantages as a search optimized data structure decreases
   i) The natural choice for representing the hyperlink relationships of web pages is undirected graph
   j) Adjacency matrix is space efficient compared with adjacency list when modeling graphs

2) Define the following in stating the principal characteristics and giving examples *(20 Marks)*
   a) Collection
   b) Random access collection
   c) Sequential access collection
   d) Group collections
   e) Binary search tree

3) a) Write a console C# program to track the sales per day of two months: January (31 days) and February (29 days) using a jagged array. The program should read the sales for the two months from the console then calculates and prints the average sales per day in each month. The program should also calculate the global average sales per days during the two months. *(10 Marks)*
   b) Explain the idea of the Big-Oh analysis, then give some rules for its application to get the execution time complexity for an algorithm written in C# *(10 Marks)*

4) a) Write a C# program that implement and test the sequential search algorithm. Design the algorithm so that it optimizes the data to make searching the frequently searched data faster in two different ways *(10 Marks)*
   b) Write a C# class that implement a priority queue that stores elements. Each element has a name and a priority represented as an integer number. Small number means

high priority and greater number means low priority. You can base your implementation on the generic queue in the .Net class library *(10 Marks)*

5) a) For the binary tree given in figure a below, Write the node values in the tree in traversing the tree in the following manners *(5 Marks):*
   i) Preorder traversal
   ii) Inorder traversal
   iii) Postorder traversal

   b) Write a C# function that accepts a binary tree root node and removes all the leaf nodes from the tree. Write a C# console program that demonstrate the operation of the function using the tree shown in figure a below by doing the following *(15 Marsk):*
   i) Building the binary tree shown
   ii) Print out the maximum depth of the tree using the function built in problem 1
   iii) Execute the function to remove all the leaf nodes from the tree
   iv) Re-print out the maximum depth of the tree to show the new maximum depth value of the tree after removing all the lead nodes

   c) All nodes along children pointers from root to leaf nodes form a path in a binary tree. Given a binary tree and a number, write a C# program that prints out all of paths where the sum of all nodes value is same as the given number. For instance, if inputs are the binary tree in figure b below and a number 22, two paths with be printed: One is the path contains node 10 and 12, and the other contains 10, 5 and 7. *(10 Marks)*

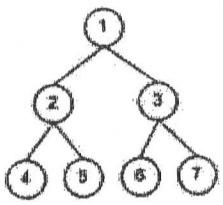

Figure a

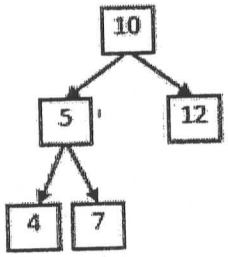

Figure b

Best wishes

Tanta University	Department: Computer and Control Engineering Total Marks: 75 Marks	Faculty of Engineering
Course Title: Microprocessors Date: January 2014(First term)	Course Code: CCE2108 Allowed time: 3 hrs	Year: 2nd No. of Pages: (2)

Answer the following problems

Problem number (1) (18 Marks)

[a] Put (✓) or (x), then write correct statement **(11Marks)**

1) A bus is set of common connection lines that carry the same type of information.
2) In real mode, the code segment is limited to 64 Kbytes in 80386.
3) In real mode, segments can begin at any location in the memory system.
4) PUSH BX is equivalent to PUSH EBX
5) MOV CX, DL
6) STD
7) MOV CS, BX
8) PUSH 73_H
9) LES BX, CAT
10) LEA CX,[BL]
11) IN DX
12) REP STOSW
13) AND AL, BL

[b] Draw the internal architecture of the microprocessor 80286, then describe the use of all registers. (7 Marks)

Problem number (2) (17 Marks)

[a] For the following instructions determine the data addressing mode and define its function. (9 Marks)

1) MOV $[1234_H]$, BX
2) DIV CH
3) ADD CL, [BX + DI]
4) INC BYTE PTR[BX]
5) MOV ARRAY[BX], AX
6) MOV [BX], DH

[b] Comparison between: (8 Marks)

1) The real mode operation and the protected mode operation.
2) The 16-bit instruction mode and the 32-bit instruction mode.
3) LOOP instruction and JMP instruction.

Problem number (3) (20 Marks)

[a] In a machine language instruction, what is specified by the MOD field, the D and W bits found in some machine language instructions. (6 Marks)

[b] If a MOV SI, [BX +DI+ 20_H] instruction appears in a program, what is its machine language equivalent? (6 Marks)

Op-code MOV is 22_H			
R/M code	Addressing mode	Code	REG field
000	DS: [BX + SI]	011	BX
001	DS: [BX + DI]	110	SI
111	DS: [BX]	111	DI

[c] Describe the operation of each of the following instructions and the content of the BX in each instruction after execution assuming the initial values are DS = 0200_H, BX = $4F82_H$ (8 Marks)

1) INC BX
2) SUB BH, 20_H
3) ROR BX, 2
4) AND BX,$F0FF_H$

Problem number (4) (20 Marks)

[a] Suppose that DS = 0400_H, BX = 0300_H, SS = 0200_H, SP = 0001_H, and DX= 0600_H. Determine the memory address accessed by each of the following instructions and its content, assuming real mode operation: (8 Marks)

1) MOV [0700_H], BX
2) PUSH BX
3) MOV [BX].DX
4) INC BYTE PTR[BX]

[b] Explain the meaning of the following instructions: (12 Marks)

1) . MODEL SMALL
2) PUSHA
3) MOV BX, OFFSET DATS
4) CMOVS BX, DX
5) OUT DX, AX
6) OUTSB
7) DATAS DW 20_H
8) MUL DI

مع أطيب الأمنيات بالتوفيق

TANTA UNIVERSITY
Electrical Power and Machines Engineering Department
Faculty Of Engineering

FINAL EXAM 2013/2014 – First Term

Course	Energy conversion (EPM2143)	Time	3 hours
Students	2nd Year (Computer and Control Engineering)	Mark	70
Date	4 / 1 / 2014	Number of pages	2

Answer ALL the following questions:

The first question (14 marks)

A	Draw and explain load characteristics of d.c. compound generator.
B	A 50 kW, 250 V series generator has an armature resistance of 0.02Ω and series field resistance of 0.045Ω The mechanical losses are 2.5 kW. At rated load Calculate: a) Armature current. b) Generated voltage. c) Armature copper losses. d) Field copper losses. e) The generator efficiency.

The second question (14 marks)

A	Explain the various methods of speed control of d.c shunt motor.
B	A 200 V d.c shunt motor has an armature winding resistance of 0.1 Ω and the shunt field resistance is 400 Ω. When the motor draws a supply current of 10A, the rotational loss is 100W and the speed is 400rpm. Find. a- The developed power. b- The net output power. c- The motor efficiency. d- The net output torque. f- If the flux is halved while the armature current is maintained constant. Find the new speed for the same supply voltage g- If the torque is doubled, find the new speed for the same supply voltage.

The third question (14 marks)

A	Explain the short circuit test and open circuit test on transformer. Why these tests are to be performed?

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B	A 2500/250 V, 50 Hz, 50 kVA, single-phase transformer has a resistance of 0.8 ohm and 0.012 and a reactance of 4 ohm and 0.04 ohm for high and low voltage windings respectively. Transformer gives 0.96 maximum efficiency at 0.75 full-load at unity power factor. The magnetization component of no-load current (I_m) is 1.2 A on 2500 V side. Find out ammeter, voltmeter and wattmeter readings on open circuit and short circuit test, if supply is given to high voltage side in both cases.
The fourth question (14 marks)	
A	Discuss briefly the starting methods of a three-phase induction motor.
B	A 480 V, 60 Hz, 50-hp, three-phase induction motor is drawing 60 A at 0.85 power factor lagging. The stator copper losses are 2000 W, and the rotor copper losses are 700 W. the friction and windage losses are 600 W, the core losses are 1800 W. find the following quantities: a- The air gap power b- The power converted P_m c- The output power P_{out} d- The efficiency of the motor
The fifth question (14 marks)	
A	What conditions are necessary for paralleling two synchronous generators?
B	A 200 V, three-phase star-connected round rotor synchronous generator gives on open circuit, e.m.f of 200 V, for afield current of 0.35 A. the same field current on short circuit causes an armature current of 12 A. the armature resistance measured between two lines is 1.8 ohm. Find the regulation for the current of 10 A at 0.9 lagging and 0.7 leading power factors.

Good Luck and best wishes
Dr. Abd El-Wahab Hassan

(2/2)

Tanta University

Department: Computers and Automatic Control Eng.
Total Marks: 90 Marks

Faculty of Engineering

Course Title: **Digital Systems**	Course Code: **CCE2107**	Year: 2nd Computers
Date: **Jan. 22nd 2014 (First Term)**	Allowed time: **3 hrs**	No. of Pages: (3)

Remarks: **Please Read the question more than once to fully understand it before you start solving, Do not forget to make verification and validation for your answers.**

Problem number (1) (30 Marks)

a) Differentiate between Mealy and Moore state machine? Draw an example for both using state diagrams and circuit diagrams.

b) Compare Synchronous and Asynchronous reset. Show how to perform both (use also a diagram to illustrate your answer.

c) What is a Johnson counter? How many unused states are present? Draw the circuit and write down the state used in sequence. What is the relation between each count and the next one?

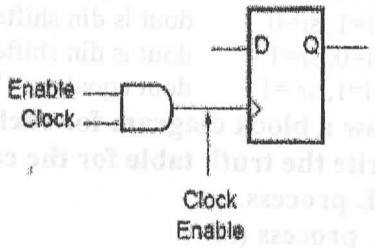
d) How can you convert a JK flip-flop to a D flip-flop? Prove your answer and draw the circuit.

e) Minimize the states shown in the following table. Draw the state diagram for the circuit before and after minimization

Present State	Next State / Output			
	00	01	10	11
A	I/0	B/1	C/0	E/0
B	G/0	C/0	H/0	D/0
C	A/0	D/0	F/0	H/0
D	I/0	F/0	E/0	B/0
E	C/0	D/0	I/0	G/0
F	G/0	B/0	C/0	E/0
G	G/0	D/1	F/0	H/0
H	F/0	B/0	G/0	A/0
I	A/0	B/1	C/0	E/0

Problem number (2) (30 Marks)

a) Explain how this circuit works and draw its timing diagram.



b) Design a counter with the following binary sequence 0, 1, 9, 3, 2, 8, 4 and repeat. Use T flip-flops.

c) Give the excitation tables of JK, D and T flip-flops and state when and how to use them.

d) A sequential circuit has three D flip-flops X, Y, Z, and one input W. The circuit is described by the following input equations:

$DX = (YZ' + Y'Z)W + YZW$

$DY = X$ $\qquad$ $DZ = Y$

(1) Draw the logic circuit. (2) Derive the state table for the circuit.

(3) Draw two state diagrams, one for W=0 and the other for W=1.

Problem number (3) (20 Marks)

a) Draw the logic diagram of a 6-bit ripple binary up-counter. Give the range of numbers covered by this circuit. Comment how this circuit can be converted to a binary down-counter.

b) In the following ASM chart :

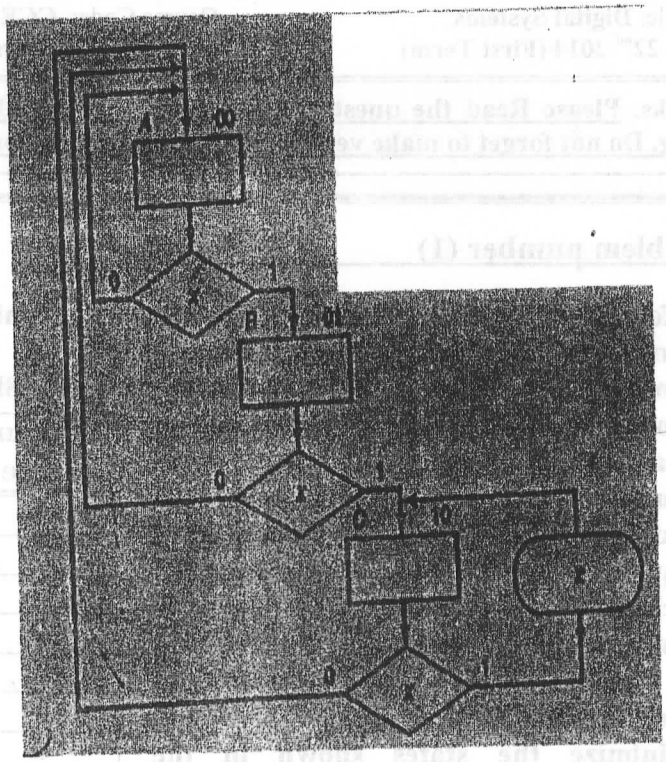
1- What are the values checked?

2- What are the operations performed in each state?

3- What is the number of states?

4- Draw the state diagram.

5- Design the control circuit using only D flip-flops. Is there any other method that is preferred to this method?



c) Why do we need a universal register? Design a universal register that performs the following operations:

1- set the output to all 1's
2- parallel load from external inputs (I's)
3- keep last value
4- shift right

Problem number (4) (20 Marks)

a) The entity declaration for a 4 bit combinational shifter block is shown below:

```
Entity myshift is
   Port (  din: in std_logic_vector(3
downto 0);
          sl:  in std_logic;
          sr: in std_logic;
          sl_in :  in std_logic;
          sr_in  : in std_logic;
          dout:  out std_logic_vector(3 downto 0)
   )
End myshift;
```

The shifter has the following functionality:

sl=0, sr= 0	:	dout equals to din
sl=1, sr=0		dout is din shifted left by 1 position, new LSB of dout is sl_in
sl=0, sr=1		dout is din shifted right by 1 position, new MSB of dout is sr_in
sl=1, sr =1		dout equals to 1's complement of din (NOT of din)

Draw a block diagram for such circuit. Write the VHDL architecture for this block.

b) Write the truth table for the combinational functional below that is described by the VHDL process.

```
process (A)
        begin
          Y1 <= '0';  Y0 <= '0';
        if (A = '1') then
            Y1 <=  '1';
        else
            Y0 <= '1';
        end if;
end process;
```

c) Write down a VHDL for 2-to-4 decoder with enable line.

d) Write the VHDL module description of a counter with an asynchronous reset (active high) signal. The counter should count from 1 to 99 on the rising edge of a clock. Once the counter gets to 99 it should restart at 1.

Good Luck

(You have 10 degrees bonus)

Course Coordinator: Assoc. Prof. Dr. Amany Sarhan

TANTA UNIVERSITY	**FACULTY OF ENGINEERING**
DEPARTMENT OF COMMUNICATIONS	**1ST SEMSTER, 2ND YEAR, 20-1-2014**
ELECTRONIC CIRCUITS & MEASUREMENTS	**TIME: 3 HOURS**
FIRST TERM EXAM	**TOTAL MARKS: 85**

Answer the following questions

Question (1)

(a) Explain -with draw- what is meant by (Negative Feedback Amplifier)? (5)

(b) State the PROS and CONS of the Feedback amplifiers. (5)

(c) An amplifier has a voltage gain of 100 and its voltage gain is increased to 200 by increasing the bias conditions. Calculate the negative feedback factor that must be applied to bring the voltage gain to the original value 100. (7)

Question (2)

(a) Explain (with DRAW) how the Hartley oscillator works. (5)

(b) What are the required conditions to sustain the oscillation of the oscillators, and what will happen if one of them is not fulfilled? (5)

(c) A Colpitts Oscillator circuit having two capacitors of 10 pF and 100 pF respectively are connected in parallel with an inductor of 10 mH. Determine the frequency of oscillations of the circuit. (7)

Question (3)

(a) Explain (with DRAW) the principle of operation of Basic BJT astable multivibrator. (6)

(b) What is meant by (Schmitt trigger)? Draw its symbol and the two-transistor Schmitt trigger circuit. (6)

(c) Compare between the different types of multivibrator. (5)

Question (4)

(a) State the most important parameters that define the performance of the RF power amplifier. (5)

(b) For a class B amplifier providing a 20 V peak signal to a 16 Ω load (speaker) and a power supply of V_{CC} = 30 V, determine the input power, output power, and circuit efficiency. (6)

(c) Calculate the efficiency of a transformer-coupled class A amplifier for a supply of 12 V and outputs of :

(i) V (p) = 12 V.

(ii) V (p) = 6 V.

(iii) V (p) = 2 V. (6)

Question (5)

(a) State the four different types of ac voltage controllers. (5)

(b) State 4 applications of AC Voltage Controllers. (4)

(c) A single phase full wave ac voltage controller working on ON-OFF control technique has supply voltage of 230 V, RMS 50 Hz, load = 50 Ω. The controller is ON for 30 cycles and off for 40 cycles. Calculate: (8)

(i) ON & OFF time intervals.

(ii) RMS output voltage.

(iii) Input P.F.

(iv) Average and RMS thyristor currents.

WITH BEST WISHES

Dr. Mohamed Salah

Tanta University Faculty of Engineering	(2013-2014) PME2111 Second year (Computer and Automatic Control)

Q (1) (25M)

(a) Use Lagrange polynomial to find one root of $\cosh x + x - 3 = 0$

(b) Deduce the form of Newton's divided difference low where

$F[x_{i+1}, x_i] = \frac{y_{i+1} - y_i}{x_{i+1} - x_i}$ and $F[x_{i+2}, x_{i+1}, x_i] = \frac{F[x_{i+2}, x_{i+1}] - F[x_{i+1}, x_i]}{x_{i+2} - x_i}$

(c) From the following table find

x	0	0.5	1	1.5	2	2.5	3
f(x)	2	2.7	3.1	5.2	7.2	9	11

(i) Find f(0.21), f(1. 1) and f(2. 55)
(using Newton's and Stirlling methods)

(ii) $D_{2,2}$ (Ricardson extrapolation) where $D_{1,1} = f'(1)$.

(iii) f '(1) , f ''(1), f '(0.1) and f ''(0.1) .

Q (2) (25M)

(a) Deduce the form of truncation error and the form of trapezoidal integration rule.

(b)Find an approximate value of $\int_0^2 e^{x^2} dx$ by using

(i) Trapezoidal rule (ii) Simpson rule
(iii)weddle method (v) Find $R_{2,2}$ (Romberg extrapolation)
(vi) Gauss three-pionts

(c) Use Newtons backword formula to derive Adams-Bashfourth two-step method then use it to find y(0.4) , h=0.1 for

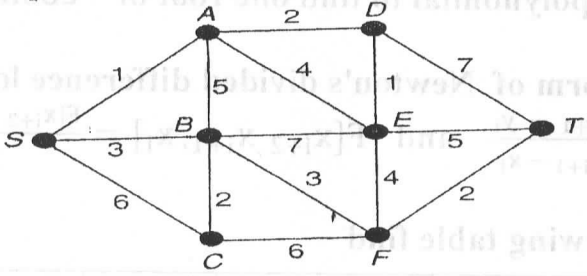
$\frac{d^2y}{dx^2} = 2x + y$ where $y(0) = 1$, $y'(0) = 0$

Q (3) (25M)

(a) Prove that if G=(V,E) is a simple graph, n is number of edges and m is a number of Vertices then $n \leq \binom{m}{2}$

(b) Show that the number of vertices of odd degree in a graph G=(V,E) always even

(c) Find the short path from S to T by Dijkstra method

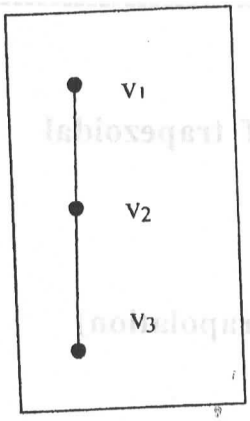


Q (4) (25M)

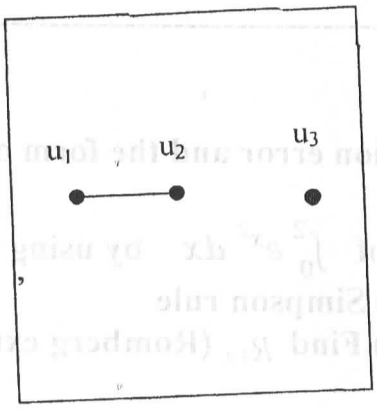
(a) Consider the graphs G≡(V1,E1), H≡(V2,E2), M≡(V3,E3)and N≡(V4,E4) find: (i) The join graph for G and H(G+H)

(ii) The product graph for two graph M and N (M X N)

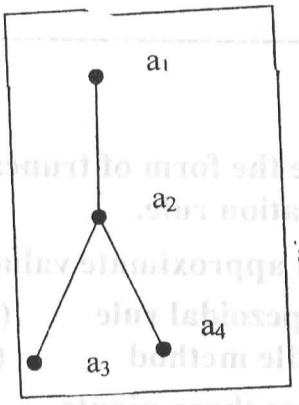
(iii) Using the adjacent matrix to show that N=(V4,E4) is connected Where V1 = {v1,v2,v3}, V2 = { u1,u2,u3}, V3 ={a1,a2,a3,a4} , V4 = {b1,b2,b3}



G ≡V_1,E_1)

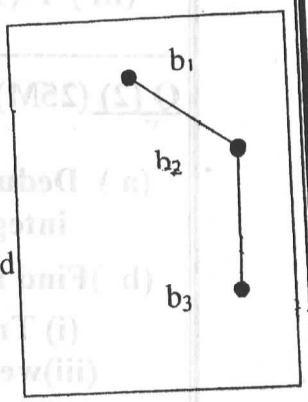


H≡V_2,E_2)



M≡ (V_3,E_3)

and



N≡(V_4,E_4)

(b) Decide whether the sequence S: 5, 4,3,3,2,2,2,1,1,1 is graphical by use deletion degree theorem

(c) Show that two graph G and H are isomorphic graphs if degrees of vertices of G and H are same.

(d) Show that in a bipartite graph G≡ (V,E) each cycle in G has even length

With my best wishes

Dr: M.Shokry